

ABSTRACT

A calibration circuit for calibrating the input data path of a digital circuit is disclosed. A simple string of a repeating data pattern such as, e.g., "1100," is
5 sent on the data path. The digital circuit captures the data using a clock signal, examines the data signal for the predetermined pattern and adjusts a delay applied to the data signal until the predetermined pattern is recognized. Then the delay is further adjusted until the predetermined pattern is no longer
10 recognized indicating that an edge of the eye of the data is near a clocking edge of the clocking signal. The delay applied to the data signal is then further adjusted by a predetermined amount to position the clock edge near the center of the data eye.